REMARKS:

Claims 1-16 are currently pending. Claims 1-11 are currently being considered, of which claim 5 has been amended. Claims 12-16 stand withdrawn from consideration.

The Examiner has indicated that claims 8 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant appreciates this indication of allowable subject matter in claims 8 and 10, and respectfully requests that the Examiner hold this objection in abeyance while considering the remarks herein regarding base claim 1.

Claims 1-7, 9, and 11 stand rejected under 35 USC 102(b) as anticipated by USP 5,559,343 (**Kiehl**).

Applicant respectfully traverses this rejection.

Kiehl discloses a semiconductor device comprising: a n-type GaAs layer (source layer) 12 formed on a semi-insulating GaAs substrate 11; a multi-layer structure of p-type A1GaAs layers 13a-13d and GaAs layers 14a-14c formed on the n-type GaAs layer 12; arsenic precipitates 21a-21c formed in the GaAs layers 14a-14c respectively; a n-type InGaAs layer 16 formed on the multi-layer structure; a WSi electrode (WSi stressor) 17 formed on the n-type InGaAS layer 16; a dielectric layer

23 of SiO_2 formed on side surfaces of a mesa structure; a drain electrode 25a formed on the WSi electrode 17; gate electrodes 25b, 25c formed on both sides of the mesa structure with the dielectric layer 23 therebetween; and a source electrode 26 connected to the n-type GaAs layer (source layer) 12 (FIGs. 8A-8G).

The precipitates 21 form Schottky contact with the GaAs layers 14 and also with the A1GaAs layers 13. Since the barrier layer 13 between adjacent pair of precipitates 21 are sufficiently narrow, a charge on one precipitate 21 can tunnel through the barrier layer 13 to the adjacent precipitate 21. Such tunneling can be controlled by potential distribution in the superlattice structure 13, 14. The potential of the precipitates 21 can be controlled by the voltage applied to the gate electrode 25b, 25c. In **Kiehl**, the tunnel current flows in a direction perpendicular to the surface of the substrate 11.

The features disclosed by the present application are clearly different from the disclosure of **Kiehl**. The present invention is clearly different from **Kiehl**.

First, in the present invention, a two-dimensional carrier gas 19 is formed in a first semiconductor layer 18 (see FIGs. 5A and 5B of the present application). The reason that the two-dimensional carrier gas 19 is formed in the first semiconductor layer 18 is for forming a channel region 29 in the first semiconductor layer 18 (see FIGs. 1 to 2B of the present application).

The Examiner states that "as **Patel et al.** 5,701,017 makes clear at column 1 lines 10-31, a 2DEG is always formed at the interface between a doped AlGaAs barrier layer such as Kiehl's layer 13a and a GaAs layer such as **Kiehl's** layer 14a" (Office Action dated July 1, 2005, page 6).

However, in **Kiehl**, the tunnel current flows in the direction perpendicular to the surface of the substrate 11. In **Kiehl**, a two-dimensional carrier gas does not function as a pass of a current, even if the two-dimensional carrier gas is formed in the interface between the p-type AlGaAs layer 13a and the GaAs layers 14. Therefore, it is irrelevant to the present invention whether the two-dimensional carrier gas is formed or not in **Kiehl**.

Second, in the present invention, oxide layers 26a, 26b are formed on both sides of a dot-shaped structure 24 on the <u>upper surface</u> of the second semiconductor layer 22 (see FIGs. 1 to 2B of the present application).

On the other hand, in **Kiehl**, the dielectric layer 23 is formed on the <u>side surfaces</u> of the GaAs layer 14b (see FIG. 8G of **Kiehl**).

The dielectric layer 23 of **Kiehl** does <u>not</u> correspond to the oxide layers 26a, 26b of the present invention.

In the present invention, since the oxide layers 26a, 26b are formed on the upper surface of the second semiconductor layer 22, it is possible to form depletion regions 28a, 28b in the first semiconductor layer 18 below the oxide layers 26a, 26b. Therefore, in the present invention, it is possible to define a channel region 29 by the depletion regions 28a, 28b.

Kiehl fails to describe, teach, or suggest such features of the present invention. The dielectric layer 23 of **Kiehl** is for insulating the gate electrodes 25b, 25c from the multi-layer structure of the p-type AlGaAs layers 13a-13d and the GaAs layers 14a-14c. The dielectric layer 23 of **Kiehl** is <u>not</u> for forming a depletion region in the GaAs layer 14a.

Third, all of precipitates 21a-21c of **Kiehl** function as a pass of tunnel current when the tunnel current flows in the multi-layer structure of the p-type AlGaAs layers 13a-13d and the GaAs layers 14a-14c. Therefore, the precipitate 21a is formed <u>in</u> the GaAs layer (first semiconductor layer) 14a, and the precipitate 21b is formed <u>in</u> the GaAs layer (second semiconductor layer) 14b (see FIG. 8B of **Kiehl**). Since the functions of the precipitates 21a-21c are the same each other, it is not necessary to make a plurality of precipitates. As shown in FIG. 15A, a number of the precipitate 21 can be only one.

On the other hand, a quantum dot 20 of the present invention is for control the transport of a carrier in a two-dimensional carrier gas 19 formed in a first semiconductor layer 18. Therefore,

the quantum dot 20 of the present invention is formed over the first semiconductor layer 16 (see FIG. 1 and 2A of the present application). The function of the quantum dot 20 of the present invention is different from the function of the precipitate 21a of **Kiehl**. Furtheremore, position of the quantum dot 20 of the present invention is different from the position of the precipitate 21a of **Kiehl**. Therefore, the quantum dot 20 of the present invention does not correspond to the precipitate 21a of **Kiehl**.

In the present invention, the function of a dot-shaped structure 24 is a mark when the oxide layers 26a, 26b are formed on the upper surface of the second semiconductor layer 22. Therefore, the dot-shaped structure 24 of the present invention is formed on the surface of the second semiconductor layer 22 (see FIG. 1 and 2A of the present application). The function of the dot-shaped structure 24 of the present invention is different from the function of the precipitate 21b of **Kiehl**. Furthermore, position of the dot-shaped structure 24 of the present invention is different from the position of the precipitate 21b of **Kiehl**. Therefore, the dot-shaped structure 24 of the present invention does not correspond to the precipitate 21b of **Kiehl**.

As described above, the present invention is clearly different from **Kiehl**.

Kiehl fails to describe, teach, or suggest the following features set forth in claim 1: "A quantum semiconductor device comprising: a first semiconductor layer formed over a substrate and

having a two-dimensional carrier gas formed in; a quantum dot formed over the first semiconductor layer; a second semiconductor layer formed over the first semiconductor layer, burying the quantum dot; a dot-shaped structure formed on the surface of the second semiconductor layer at a position above the quantum dot; and oxide layers formed on both sides of the dot-shaped structure on the upper surface of the second semiconductor layer", in combination with the other claimed features.

Kiehl fails to describe, teach, or suggest the following features set forth in claim 11: "A method for fabricating a quantum semiconductor device comprising the steps of: forming over a substrate a first semiconductor layer with a two-dimensional carrier gas formed in; forming a quantum dot over the first semiconductor layer; forming a second semiconductor layer, burying the quantum dot; forming a dot-shaped structure on the surface of the second semiconductor at a position above the quantum dot due to strains generated in the surface of the second semiconductor layer due to the presence of the quantum dot; and forming oxide layers on the upper surface of the second semiconductor layer on both side of the dot-shaped structure with the dot-shaped structure as a mark", in combination with the other claimed features.

Kiehl fails to describe, teach, or suggest the features set forth in base claims 1 and 11, and therefore **Kiehl** also fails to describe, teach, or suggest the features set forth in all claims depending therefrom.

Thus, Applicant respectfully submits that the rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, it is respectfully submitted that all claims currently being considered are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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